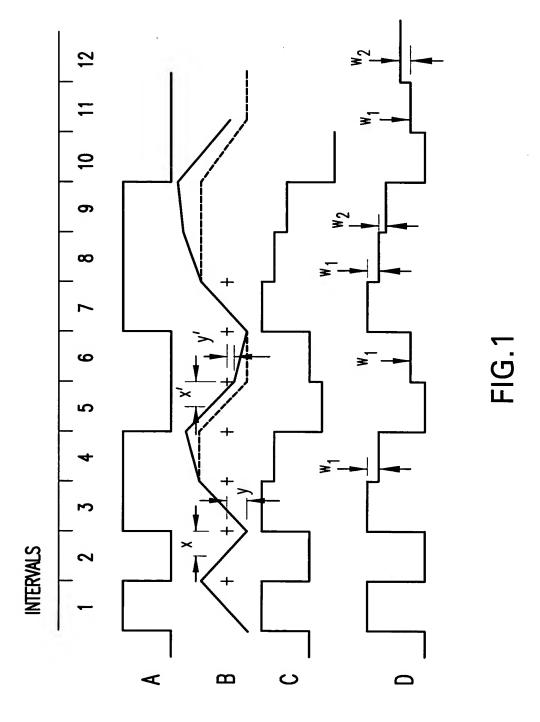
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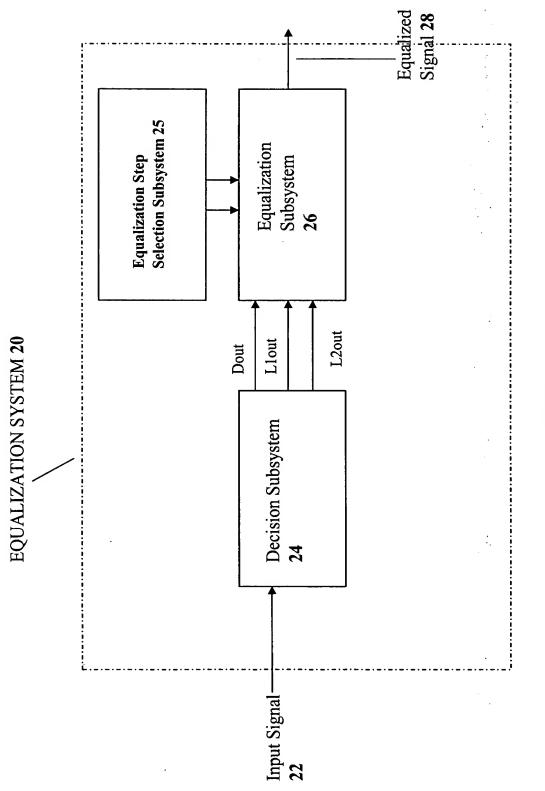


Fig. 2

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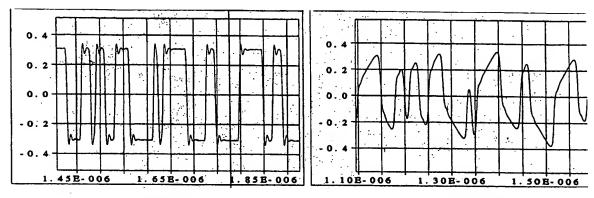


Fig. 3(a) Fig. 3(b)

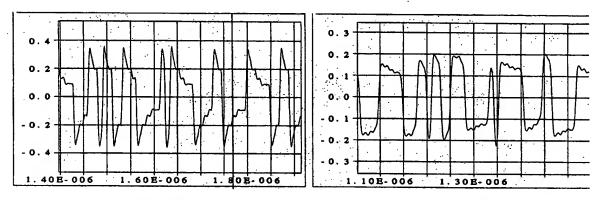
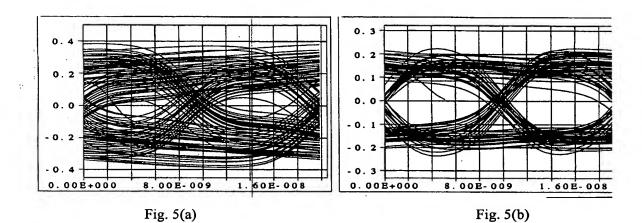


Fig. 4(a)

Fig. 4(b)

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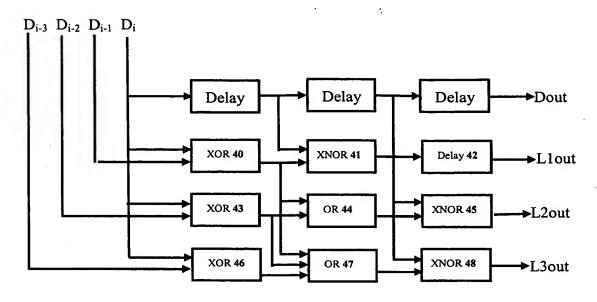


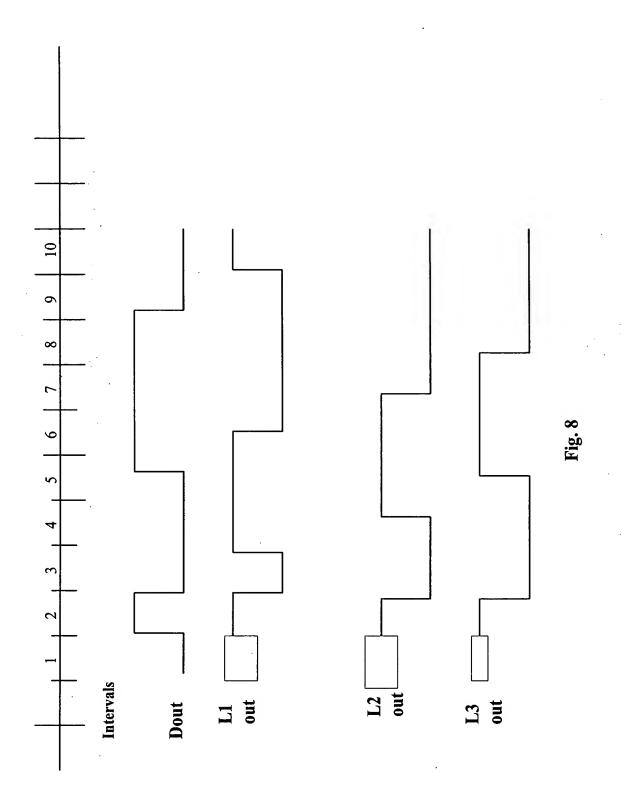
Fig. 6 A block diagram for the equalization logic that generates the three signals levels

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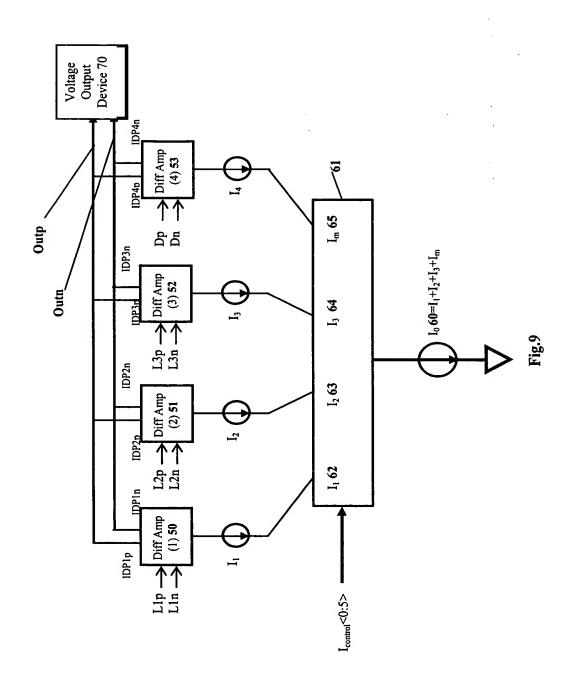
Sample Input Stream = 01000111100 (a = MSB; b = first to right of MSB; k = LSB) a = 0; b = 1; c = 0; d = 0; e = 0; f = 1; g = 1; h = 1; l = 1; j = 0; k = 0

| Bit Identity | Dout | L1out | L2out | L3out |
|--------------|------|-------|-------|-------|
| а | 0 | | | |
| b b | 1 | 1 | 1 | 1 |
| С | 0 | 0 | 0 | 0 |
| d | 0 | 1 | 0 | 0 |
| e | 0 | 1 | 1 | 0 |
| f | 1 | 4 | | |
| | | | 1 | 1 |
| g | 1 | 0 | 1 | 1 |
| h h | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| jj | 0 | 0 | 0 | 0 |
| k | 0 | 1 | 0 | 0 |

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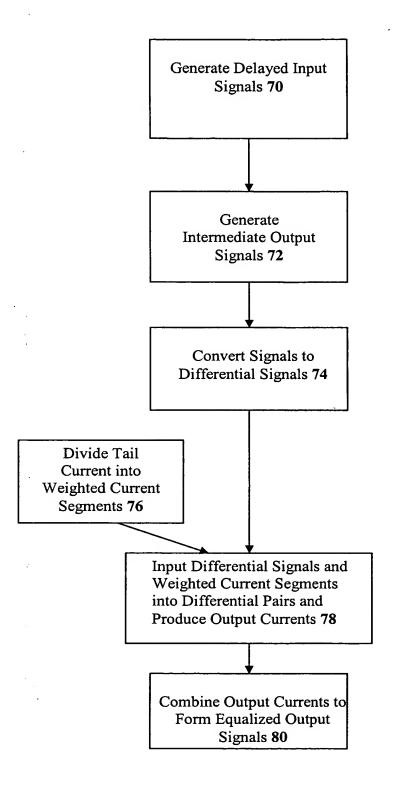


Fig. 10